# PURDUE PETE

1727 Linden Avenue
New Albany, IN 47150
(812) 941-4781
E-mail: P.Pete@purdue.edu

**OBJECTIVE**

Seeking an internship in electrical engineering with Samtec, Inc.

**EDUCATION**

Bachelor of Science, Electrical Engineering Technology (May 20XX) GPA: 3.37/4.00
Purdue University, College of Technology at New Albany

Tools: Microsoft Office Programs, ClearCase, Orcad Pspice Schematic, Alterra Max Plus Software

Academic Projects:

Design of a 4 Bit Processor

- Designed and implemented a 4 bit processor using Alterra Max Plus Schematic design environment
- Included a processor with an ALU which could do arithmetic as well as logical operations
- Implemented a Von Neumman architecture where the program and data memory were in the same space

Multi-Objective Optimization using Genetic Algorithms

- Implemented two genetic/evolutionary algorithms in order to simultaneously optimize multiple objective functions
- Designed the initial "population" of solutions which were randomly chosen and evaluated based on their corresponding values in the objective functions
- Applied a selection scheme to determine "parents", performed crossover and Mutation, and created a new population
- Repeated this process for a number of "generations" until the optimal solutions dominated the population

Amateur Radio Operator License – May 20XX

**EXPERIENCE**

Freescale Semiconductor Austin, TX May 20XX – Aug 20XX
*Engineering Rotation Program*

- *Product Engineering* – Analyzed statistics of probe and final test wafer fallout with a focus on yield enhancement. Correlated this data to fab class probe parameters for process improvement.
- *Audio, Image, and Video Software Development* – Analyzed PMP architecture to develop and implement an adaptive clock algorithm in order to ensure skipfree media playback while providing minimal power consumption.

**EXPERIENCE, continued.**

Freescale Semiconductor Austin, TX May 20XX – Aug 20XX
*Design Verification Intern*

- Performed standalone design verification using verilog. Wrote functional verification, code coverage, and regression on the standalone design.

Freescale Semiconductor Austin, TX May 20XX – Aug 20XX
*Manufacturing Engineer Intern*

- Operated the J750 wafer prober performing probe testing and postprobe process inspection including examination and characterization of die pad defects.

**EXTRA-CURRICULAR ACTIVITIES**

President IEEE Student Chapter, Sept. 20XX - Present

- Organized speaker's bureau for chapter meetings

Organizational Vice President IEEE Student Chapter, Sept. 20XX – Aug 20XX

- Established student chapter at Indiana University Southeast as member of organizational team
- Presided over meetings in absence of president

American Collegiate Minute Men, Sept. 20XX - Present

- Coordinated events Coordinator

Student Leadership Program, Jan. 20XX-May 20XX

Community Service (Goodwill, American Heart Walk, Annual River-Walk Clean-up)

Contributor to Make Magazine

**COMPUTER SKILLS & PROGRAMMING LANGUAGES**

C/C++, Verilog/System Verilog, Linux, Command Line, Motorola 68K Assembly, Matlab Veritex, Ladder Logic, XML, Perl, Tcl

**REFERENCES**

Available on request

.